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08/056,301 04/30/93 SLEMMER

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EXAMINER CUNNINGHAM, T
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B5M1/0404

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ART UNIT	PAPER NUMBER
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2504

DATE MAILED: 04/04/95

This is a communication from the examiner in charge of your application.  
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☐ Responsive to communication filed on \_\_\_\_\_ ☐ This action is made final.

A shortened statutory period for response to this action is set to expire three month(s), \_\_\_\_\_ days from the date of this letter.  
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

**Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:**

- |   |  |
|---|--|
| 1. <input checked="" type="checkbox"/> Notice of References Cited by Examiner, PTO-892. | 2. <input checked="" type="checkbox"/> Notice of Draftsman's Patent Drawing Review, PTO-948. |
| 3. <input checked="" type="checkbox"/> Notice of Art Cited by Applicant, PTO-1449.      | 4. <input type="checkbox"/> Notice of Informal Patent Application, PTO-152.                  |
| 5. <input type="checkbox"/> Information on How to Effect Drawing Changes, PTO-1474.     | 6. <input type="checkbox"/> _____  |

**Part II SUMMARY OF ACTION**

1. ☒ Claims 1-26 are pending in the application.  
Of the above, claims \_\_\_\_\_ are withdrawn from consideration.
2. ☐ Claims \_\_\_\_\_ have been cancelled.
3. ☐ Claims \_\_\_\_\_ are allowed.
4. ☒ Claims 1-26 are rejected.
5. ☐ Claims \_\_\_\_\_ are objected to.
6. ☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.
7. ☒ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.
8. ☐ Formal drawings are required in response to this Office action.
9. ☐ The corrected or substitute drawings have been received on \_\_\_\_\_. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).
10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on \_\_\_\_\_, has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).
11. ☐ The proposed drawing correction, filed \_\_\_\_\_, has been ☐ approved; ☐ disapproved (see explanation).
12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. \_\_\_\_\_; filed on \_\_\_\_\_.
13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.
14. ☐ Other

**EXAMINER'S ACTION**

Art Unit 2504

The disclosure is objected to because the described operation of the circuit shown in Figs. 2 and is not clearly understood. Page 12, line 11, states that "the sum of the currents at node VSUM may be set equal to zero" (underlining added). This statement is not clearly understood because according to Kirchoff's current, the current into any node at any given time must be equal to zero. The sizes of the transistors used should not and cannot effect the sum of the current at the summing node. It would be clearly understood by one skilled in the art that the sizing of the transistors can only affect the level of the voltage at the summing node VSUM, not the current. Appropriate correction is required.

The Abstract is objected to for similar reasons as discussed above with the specification. Appropriate correction is required.

Claims 1-26 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, line 7, similarly as discussed above, it is not understood how the "current at the summing node" can be "equal to zero" only "when the power supply voltage is equal to a preselected voltage", when it is clear from Kirchoff's current law that such will always be equal to zero.

The language of claim 2 is considered to be vague.

In claim 3, there is no antecedent for "the threshold voltage" or "the base emitter voltage". Also, in lines 5 and 6, it is not understood how " $kT/q$ " can be "the threshold voltage". Firstly, a "threshold voltage" has already been recited in line 4. And secondly, this statement does not find support in the specification.

In claim 4, there is no antecedent for "the plurality of current mirrors". It appears that "mirrors" should be changed to --sources--.

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In claim 5, line 5, it is not understood what is meant by "a threshold voltage in the first current mirror". Just stating that the "threshold voltage" is in the "first current mirror" is vague and confusing.

Claims 6 and 7 are rejected for similar reasons as claim 5.

Claim 8 is rejected for the reasons discussed above with claims 1-7.

In claim 9, there is no support found in the specification for a "clamping circuit" which is "connected to the summing node". Also, it is not understood how a "voltage swing" can be "selected".

In claim 10, it is not understood what is meant by "interposed". The term "interposed" has no meaning in an electrical circuit context.

Claims 11-13 are rejected for the reasons discussed above with claims 1-8.

Claims 14-26 are rejected for similar reasons as claims 1-11.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. §102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —  
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 14-16 and 18 are rejected under 35 U.S.C. §102(b) as being anticipated by Bingham. Bingham discloses, in Figs. 1 and 3, a circuit comprising: "a first circuit (20 of Fig. 1)"; "a direct current sum bandgap voltage comparator (36 and 56 of Fig. 3)" having "a summing node (52 of Fig. 3)", "a plurality of current sources (110 and 116 of Fig. 3)" and "an indicator circuit (56 of Fig. 3)"; "a switching circuit (40 and 48 of Fig. 3)"; "a primary power supply (14 of Fig. 1)"; and "a secondary power supply (22 of Fig. 1)", all connected and operating similarly as recited by Applicant.

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Claims 4-13, 17 and 19-26 would be allowable if rewritten to overcome the rejection under 35 U.S.C. § 112 and to include all of the limitations of the base claim and any intervening claims.


The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

It is noted that all the references cited on the form PTO-1449 have been considered, however, some have been lined through because they are not considered relevant enough to print on the patent at the time of issue.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Terry Cunningham at telephone number (703) 308-4872.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956.

**TC**  
**March 29, 1995**

  
**Terry D. Cunningham**  
**Patent Examiner**  
**Group Art Unit 2504**